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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/177,572	10/23/1998	YOSHIHIRO TERASHIMA	35.C13035	3325

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EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/177,572	TERASHIMA ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is made in response to applicant's amendment filed on March 08, 2005. Claims 1-16 are cancelled, claim 17 is amended, and claims 17 and 18 are currently pending in the application. An action follows below:

Drawings

2. The drawing was received on 05/21/2004. This drawing is acknowledged and approved.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwata et al (US 5,900,857) in view of Iwasaki (US 4,745,485).

5. As to claim 17, Kuwata et al teach a memory controller comprising

a writing FIFO 2 (a first FIFO section, fig. 1) storing the image data of "a" x "2n"-bit width, where "a" is a size of the inputted bit width, "n" is a positive integer number, and 2 x "n" makes an even bit (see col. 13, lines 61-67, a capacity required for DRAM 3 is 3x5x138,240=2,073,600 bits);

a DRAM 3 (a frame memory section, fig 1), a reading FIFO 5 (a second FIFO section, fig. 1);

Kuwata et al further teach, referring to col. 48, lines 44-48, input picture image data R, G, B of one frame in which pixel is constituted by 6 bits are inputted to a frame modulation/dither circuit (1). The frame modulation/dither circuit (1) produces R, G, B display data R1, G1, B1, each having 1 bit and the other data R2, G2, B2 each having 1 bit based on an input image data of 6 bits, and stores the data temporarily in FIFO2. Accordingly, a bit width of the image data stored in FIFO2 of Kuwata et al is 3/6 (1/2) of the bit width of the input image data, and would be "a" / "2n". Thus, Kuwata meets the limitation of *the image data is read out from...written into said frame memory section, and read out from said frame memory section, at a rate that is half "3/6 (1/2)" of a rate at which the image data.*

the writing FIFO 2 (the first FIFO section, fig. 1) is of a size suitable for storing image data so that, within a period for inputting the image data in the writing FIFO 2 (the first FIFO section, fig. 1) to FULL capacity (col. 13, lines 61-67, a capacity required for DRAM 3 is 3x5x138,240=2,073,600 bits). A memory control section 9 (fig. 1) and a memory control section 4 (fig. 1) perform the function of writing the image data into the frame memory, reading out the image data from the frame memory and executing a command of frame memory section are conducted (see detail in col. 11, lines 59 through col. 12, lines 27).

Accordingly, Kuwata et al teaches all of the claimed limitations of claim 17, except for "...a serial/parallel conversion...wherein the image data is read out from...written into said frame memory section, and read out from said frame memory section, at a rate that is half of a rate at which the image data..."

However, Iwasaki teaches a related memory controller which includes a serial/parallel conversion 2 (see figure 1).

Further, Iwasaki teaches "more specifically, the writing time and the reading time for one frame are equal and in the reading operation, for the upper display are 11, the video signal of the frame being presently written is read out and for the lower display area 12, the video signal one frame ahead thereof is read out. Since the picture signal is applied to the driver 9 at a speed equal to a half of the writing speed to the frame memories 4 and 5" (see col. 5, lines 55-63), as best understood.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute the serial/parallel conversion (2) taught by Iwasaki for Kuwata's frame modulation dither circuit (1) and to modify Kuwata's frame memory (DRAM 3) including half speed of write into and read out from the frame memory, in view of the teaching in Iwasaki's reference because these would provide the picture that is represented stably even if it is a moving picture as taught by Iwasaki (col. 5, lines 65-66).

6. As to claim 18, Iwasaki teach a liquid crystal panel 10, a decoder 31, and the memory controller 18 (see figure 7).

Response to Arguments

7. Applicant's arguments see pages 4 and 5, filed March 8, 2004 have been fully considered but they are not persuasive.

8. In response to applicant's argument states that claim 17 recites "the image data is read out from said first FIFO section, written into said frame memory section at half of

a rate at which the image data is inputted into said converter section, and read out from said frame memory section at a rate that is half of a rate at which the image data is inputted into said first FIFO section."

Examiner is not convinced by Applicant's argument. As stated *supra* with respect to claim 17, Examiner finds that the combination of Kuwata et al teach, referring to col. 48, lines 44-48, input picture image data R, G, B of one frame in which pixel is constituted by 6 bits are inputted to a frame modulation/dither circuit (1). The frame modulation/dither circuit (1) produces R, G, B display data R1, G1, B1, each having 1 bit and the other data R2, G2, B2 each having 1 bit based on an input image data of 6 bits, and stores the data temporarily in FIFO2. Accordingly, a bit width of the image data stored in FIFO2 of Kuwata et al is 3/6 (1/2) of the bit width of the input image data, and would be "a" / "2n", as modified by Iwasaki, teaches the claim 17 limitation of the frame memories can be formed with a total capacity corresponding to one frame (see col. 2, lines 8-9).

For these reasons, the rejections based on Kuwata et al and Iwasaki have been maintained.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KMN
June 14, 2005

XIAO WU
PRIMARY EXAMINER